Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the Claims

1. (original): A power supervision circuit for providing a logic LOW voltage at an output node when a supply voltage is below a predetermined level comprising:

an input node coupled to said supply voltage;

a first sub-circuit that allows current from said output node to flow into said ground terminal when said supply voltage is above a first voltage threshold;

a second sub-circuit that allows current from said output node to flow into said ground terminal when said supply voltage is above a second voltage threshold, wherein said second voltage threshold is greater than said first voltage threshold; and

a control node, wherein said output node is pulled-up to a logic HIGH voltage when a logic HIGH voltage is applied to said control node.

2. (original): The circuit of claim 1 wherein said first voltage threshold is less than 0 volts.

3. (original): The circuit of claim 1 wherein said second voltage threshold is greater than 0 volts.

4. (original): The circuit of claim 1 wherein said first sub-circuit comprises at least one first NMOS transistor, wherein the turn-ON voltage of said at least one first NMOS transistor is substantially equal to said first voltage threshold.

5. (original): The circuit of claim 1 wherein said second sub-circuit comprises at least one second NMOS transistor, wherein the turn-ON voltage of said at least one second NMOS transistor is substantially equal to said second voltage threshold.

6. (original): The circuit of claim 1 further comprising:

a third sub-circuit that allows current to flow from said output node to said ground terminal when said supply voltage is above a third voltage threshold, wherein said third voltage threshold is greater than said second voltage threshold.

7. (original): The circuit of claim 6 wherein said third voltage threshold is approximately 0.7 volts.

8. (original): The circuit of claim 6 wherein said third sub-circuit comprises at least one third NMOS transistor, wherein the turn-ON voltage of said at least one third NMOS transistor is substantially equal to said third voltage threshold.

9. (original): The circuit of claim 1 further comprising a current mirror coupled to said first sub-circuit.

10. (original): The circuit of claim 1 further comprising an electrostatic discharge cell coupled to said first and second sub-circuits.

11. (original): A circuit for pulling-down an output node comprising:

an input node;

a ground terminal;

a first sub-circuit coupled to said input node, said ground terminal, and said output node, said first sub-circuit comprising:

a first NMOS transistor having a first voltage threshold;

a second NMOS transistor in a compound configuration with said first NMOS transistor, wherein said second NMOS transistor has a second voltage threshold substantially equal to said first voltage threshold and said first sub-circuit provides a first current path from said ground terminal to said output node when said first and second NMOS transistors are ON; and

a second sub-circuit coupled to said input node, said ground terminal, and said output node, said second sub-circuit comprising:

a third NMOS transistor having a third threshold voltage that is greater than said first and second voltage thresholds, wherein said second sub-circuit provides a second current path from said ground terminal to said output node when said third NMOS transistor is ON.

12. (original): The circuit of claim 11 wherein said first and second voltage thresholds are less than 0 volts.

13. (original): The circuit of claim 11 wherein said first and second voltage thresholds are greater than 0 volts and less than 0.3 volts.

14. (original): The circuit of claim 11 wherein the source terminal of said first NMOS transistor is coupled to the drain terminal of said second NMOS transistor, the gate terminal of said first NMOS transistor is coupled to the gate terminal of said second

NMOS transistor, the drain terminal of said first NMOS transistor is coupled to said output node, the source terminal of said second NMOS transistor is coupled to said ground terminal, and the gate terminals of said first and second NMOS transistors are coupled to said input node.

15. (original): The circuit of claim 14 wherein the gate terminals of said first and second NMOS transistors are coupled to said input node via a resistor.

16. (original): The circuit of claim 11 wherein the drain terminal of said third NMOS transistor is coupled to said output node, the source terminal of said third NMOS transistor is coupled to said ground terminal, and the gate terminal of said third NMOS transistor is coupled to said input node.

17. (original): The circuit of claim 11 wherein the third threshold voltage is approximately 0.7 volts.

18. (original): The circuit of claim 11 further comprising a third sub-circuit coupled to said input node, said ground terminal, and said output node, said third sub-circuit comprising:

a fourth NMOS transistor having a fourth voltage threshold;

a fifth NMOS transistor in a compound configuration with said ourth NMOS transistor, wherein said fifth NMOS transistor has a fifth voltage threshold substantially equal to said fourth voltage threshold and said third sub-circuit provides a third current path from said ground terminal to said output node when said fourth and fifth NMOS transistors are ON.

19. (original): The circuit of claim 18 wherein said fourth voltage thresholds is greater than said first voltage threshold.

20. (original): The circuit of claim 18 wherein said fourth voltage thresholds is less than said third voltage threshold.

21. (original): The circuit of claim 18 wherein said fourth voltage threshold is less than said third voltage threshold and said fourth voltage threshold is greater than said first voltage threshold.

22. (original): The circuit of claim 18 wherein said fourth voltage threshold is approximately 0.3 volts.

23. (currently amended): The circuit of claim 11 further comprising a ~~control~~ pull-up transistor coupled to said first sub-circuit, wherein said output node is pulled-up when a voltage HIGH is applied to the gate terminal of said ~~control~~ pull-up transistor.

24. (currently amended): The circuit of claim 23 further comprising:

an intermediate node coupled to the gate terminals of said first, second, and third NMOS transistors; and

a resistor coupled between said intermediate node and said input node, wherein the drain terminal of said ~~control~~ pull-up transistor is coupled to said intermediate node and the source terminal of said pull-up transistor is coupled to said ground terminal.

25. (currently amended): The circuit of claim 23 further comprising a comparator circuit coupled to the

gate terminal of said ~~control~~ pull-up transistor that compares said input voltage with a minimum voltage.

26. (original): The circuit of claim 11 further comprising:

an intermediate node coupled to the gate terminals of said first, second, and third NMOS transistors; and

a resistor coupled between said intermediate node and said input node;

a first PMOS switch, wherein the source terminal of said first PMOS switch is coupled to said input node, the gate terminal of said first PMOS switch is coupled to said intermediate node, and the drain terminal of said first PMOS switch is coupled to the source terminal of said first NMOS transistor.

27. (original): The circuit of claim 11 further comprising a current mirror coupled to said first sub-circuit for controlling the amount of current at said output node.

28. (original): The circuit of claim 11 further comprising an electrostatic discharge cell coupled to said first and third sub-circuits.

29. (original): The circuit of claim 28 wherein said electrostatic discharge cell is coupled to said first sub-circuit via a first resistor, said electrostatic discharge cell is coupled to said second sub-circuit via a second resistor, and the resistance of said second resistor is less than the resistance of said first resistor.

30. (original): A circuit for pulling-down an output node comprising:

an input node;

a first sub-circuit coupled to said input node, wherein said first sub-circuit comprises;

a first NMOS transistor;

a second NMOS transistor coupled to said first NMOS transistor in series.

a second sub-circuit coupled to said first sub-circuit, wherein said second sub-circuit comprises:

a third NMOS transistor, wherein the voltage threshold of said third NMOS transistor is greater than the voltage threshold of said first and second transistors;

a fourth NMOS transistor coupled to said third NMOS transistor in series, wherein the voltage threshold of said fourth NMOS transistor is greater than the voltage threshold of said first and second transistors;

a third sub-circuit coupled to said second sub-circuit and said output node, wherein said third sub-circuit comprises a fifth NMOS transistor, and the voltage threshold of said fifth NMOS transistor is greater than the threshold voltage of said third and fourth NMOS transistors; and

a ground node coupled to said first, second, and third sub-circuits, wherein a path to said ground node is provided to said output node when any one of said first, second, and third sub-circuits are conducting.

31. (original): A power supervisor comprising:

a plurality of inputs;

an output;

a plurality of power supervision circuits, wherein each one of said plurality of power supervision

circuits is coupled to one of said plurality of inputs, each one of said plurality of power supervision circuits is coupled to said output, a logic LOW is placed on said output when the voltage of at least one of said plurality of inputs is below at least one predetermined voltage level, each one of said plurality of power supervision circuits comprising:

a first sub-circuit having a first voltage threshold; and

a second sub-circuit having a second voltage threshold, wherein said first and second voltage thresholds are different.

32. (currently amended): A power supervisor comprising:

a plurality of inputs;

a plurality of outputs;

a plurality of power supervision circuits, wherein each one of said plurality of power supervision circuits are coupled to one of said plurality of inputs, each one of said plurality of power supervision circuits is coupled to one of said outputs, each one of said plurality of power supervision circuits comprising:

a first sub-circuit having a first voltage threshold; and

_____a second sub-circuit having a second voltage threshold, wherein said first and second voltage thresholds are different~~, said one of said plurality of power supervision circuits is coupled to one of said plurality of inputs, and said one of said plurality of power supervision circuits is coupled to one of said plurality of outputs~~.

Amendments to the Drawings

The attached three sheets of drawings include amendments to FIGS. 2, 3, and 7 and replace original sheets 2, 3, and 7.

FIGS. 2 and 3 have been amended to correct inadvertent errors made by mistake and without deceptive intent. FIGS. 2 and 3 have been amended to correlate with the specification, the claims, and FIG. 4. No new subject matter has been added. FIG. 2 has been amended such that the source terminal of transistors 242 is coupled to ground terminal 299. FIG. 3 has been amended such that the source terminal of transistors 342 is coupled to ground terminal 399.

Support for the amendments appear in the specification, the claims, and FIG. 4. Particularly, the amended configuration of transistors 242 and 342 is the same as the configuration of transistor 442 of FIG. 4. Particularly, source terminal of transistor 442 of FIG. 4 is coupled to ground terminal 499 and "components 4XX are preferable the same as components 3XX for FIG. 3" and "components 3XX are preferable the same as components 2XX of FIG. 2" (applicants' spec., page 13, lines 21-22 and page 9, lines 24-25).

The amendments of FIGS 2 and 3 are also supported by portions of the specification. For example, "By turning NMOS transistor 242 ON, the voltage on intermediate node 296 is pulled to ground" (applicants' spec., page 9). Furthermore, the amended configuration is supported by the claim wherein "the source terminal of said pull-up transistor is coupled to said ground terminal" (applicants' spec., claim 24).

FIG. 7 has been amended to correct an inadvertent numbering error made by mistake and without deceptive intent. Particularly, ground terminal 199 has been renumbered as ground terminal 799.

Attachments: Replacement Sheet for FIG. 2
Replacement Sheet for FIG. 3
Replacement Sheet for FIG. 7
Annotated Sheet Showing Changes for FIG. 2
Annotated Sheet Showing Changes for FIG. 3
Annotated Sheet Showing Changes for FIG. 7